AMENDMENTS

In the Claims:

1. (Presently Amended). A switched-mode Class F power amplifier configured for parallel connection with at least one other said amplifier for combining signals output from such parallel connected amplifiers, said amplifier comprising:

   (a) an input component comprising at least one active device configured to be alternately switched by a signal input thereto to present an amplified signal corresponding to said input signal, said amplified signal constituting a low output impedance voltage source;

   (b) an output resonator component; and,

   (c) a lumped element impedance inverter connected between said input component and said output component, said impedance inverter configured for transforming said low output impedance voltage source so as to constitute a high output impedance current source, and said high output impedance current source configured for said parallel connection;

   ~~6.~~wherein negative reactive component values theoretically required by said impedance inverter are actually ~~are eliminated and effectively provided by~~ incorporate~~ding~~ ~~said values~~ into pre-selected reactive components of said input and output components.

2. (Original). A switched-mode power amplifier according to claim 1 wherein said input signal is an analog phase modulated signal.

3. (Cancelled). ~~A switched-mode power amplifier according to claim 1, wherein a source-drain parasitic capacitance across said active device is eliminated by one or more pre-selected reactive components of said input component, the value(s) of said pre-selected reactive components being pre-determined to effectively compensate for said parasitic capacitance.~~

4. (Presently Amended). A method for producing a switched-mode power amplifier~~amplifying an input signal to produce an output signal configured for parallel connection with at least one other like output signal for combining said output signals within a Chireix circuit architecture,~~, said method comprising:

   (a) designing a theoretical lumped-element impedance inverter configured to transform a low output impedance voltage source into a high output impedance current source, such ideal impedance inverter incorporating theoretically negative reactive component values;

   ~~(a)~~(b) adding an input component comprising at least one active device configured to be alternately switched by an input signal thereto to present an amplified signal corresponding to said input signal, said amplified signal constituting a low output impedance voltage source;

(c) adding an output resonator component; and

(d) adjusting values of one or more elements coupled to the input and output components such that the theoretically negative reactive components may be eliminated, and eliminating the theoretically negative reactive components from the design.

~~providing across said active device a second harmonic resonator configured for shorting a second harmonic signal of said input signal;~~

~~(c)transforming said low output impedance voltage source to constitute a high output impedance current source by means of a lumped element impedance inverter, said high output impedance current source configured for said parallel connection; and,~~

~~(d)providing a third harmonic resonator configured for blocking a third harmonic signal of said input signal from a load connected to said output signal;~~

~~whereby negative reactive component values required by said impedance inverter are eliminated and effectively provided by incorporating said values into pre-selected adjacent reactive components of said resonators.~~

5. (Original). A method according to claim 4 whereby said input signal is an analog phase modulated signal.

6. (Cancelled). ~~A method according to claim 5 and further comprising eliminating a source-drain parasitic capacitance across said active device by one or more pre-selected reactive components of said second harmonic resonator the value(s) of which are selected to effectively compensate for said parasitic capacitance.~~

7. (Original). A plurality of switched-mode Class F power amplifiers in parallel connection for combining signals output from said amplifiers, said parallel-connected amplifiers comprising:

(a) an input component for each of said plurality of amplifiers, each said input component comprising at least one active device configured to be alternately switched by a signal input thereto to present an amplified signal corresponding to said input signal, said amplified signal constituting a low output impedance voltage source;

(b) a common output resonator component for said plurality of amplifiers; and,

(c) a lumped element impedance inverter for each of said plurality of amplifiers between said input component and said output component, said impedance inverter configured for transforming said low output impedance voltage source so as to constitute a high output impedance current source and said high output impedance current source configured for said parallel connection;

wherein negative reactive component values required by said impedance inverter are eliminated and effectively provided by incorporating said values into pre-selected reactive components of said input and output components.

8. (New). The switched-mode power amplifier according to claim 1, wherein the input component comprises a first inductor and a first capacitor, connected in series and electrically connected to the input of the impedance inverter.

9. (New). The switched-mode power amplifier according to claim 8, wherein the output component comprises a second inductor and a second capacitor, connected in series and electrically connected to the output of the impedance inverter.

10. (New). The switched-mode power amplifier according to claim 9, wherein the values for each of the first inductor, first capacitor, second inductor and second capacitor are selected in order to compensate for the negative reactive component values theoretically required but not otherwise included in the amplifier.

11. (New). The method of claim 4, further comprising manufacturing the switched-mode power amplifier.

12. (New). The method of claim 11, wherein the input component comprises a first inductor and a first capacitor, connected in series and electrically connected to the input of the impedance inverter.

13. (New). The method of claim 12, wherein the output component comprises a second inductor and a second capacitor, connected in series and electrically connected to the output of the impedance inverter.

14. (New). The method of claim 13, further comprising the step of selecting the values for each of the first inductor, first capacitor, second inductor and second capacitor in order to compensate for the negative reactive component values theoretically required but not present in the manufactured amplifier.

REMARKS

Claims 1-7 are currently pending in this Application. In the Office Action, Claims 1-7 were rejected.

In this Amendment and Response, Applicant amends claims 1 and 4 without any intention of disclaiming any equivalents thereof. Applicant also cancels pending claims 3 and 6, and adds new claims 8-14. Applicant asserts that no new matter is added by this Amendment. Reconsideration is respectfully requested.

Claim Rejections

Claims 1-7 were rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the written description requirement. As set forth in the Office Action: